



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/555,266	11/01/2005	Peter Fuhrmann	DE 030145	9354
65913	7590	04/01/2009	EXAMINER	
NXP, B.V.			BARON, HENRY	
NXP INTELLECTUAL PROPERTY DEPARTMENT				
M/S41-SJ			ART UNIT	PAPER NUMBER
1109 MCKAY DRIVE			2416	
SAN JOSE, CA 95131				
		NOTIFICATION DATE	DELIVERY MODE	
		04/01/2009	ELECTRONIC	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/555,266	FUHRMANN ET AL.	
	Examiner	Art Unit	
	HENRY BARON	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 1/30/2009.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-20 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____ .	6) <input type="checkbox"/> Other: _____ .

Detailed Action

**ERROR DETECTION AND SUPPRESSION IN A TDMA-BASED NETWORK
NODE**

Response to Arguments/Remarks

1. Claims 1 – 20 are pending in the application. Claims 17 – 20 are new.
2. Applicant's arguments filed 01/30/2009 have been fully considered but are not persuasive.
3. Applicant argues that all claim rejections are improper because the Office Action has failed to assert correspondence to multiple claim limitations in each of the independent claims, and because the interpretations of the cited references are erroneous. With regards to claim 1, which is directed to a communications unit, a bus monitor and a bus driver, where the communications unit and bus monitor each independently generate release signals, and where the bus driver compares the release signals, the Office Action asserted no correspondence to the bus driver, and the cited diagnostic unit does not correspond to the claimed communications unit as asserted. Specifically, the Office Action has erroneously that the diagnostic unit in the '805 reference corresponds to the claimed communications unit, and that the cited trigger" (or "retrigger") corresponds to the claimed release signal are erroneous because the cited diagnostic unit does not generate any trigger and thus does not correspond to the claimed communications unit (which generates a release signal). Further, Applicant argues, these assertions are further erroneous because the cited "retrigger" is compared to a time pattern generated by a "time registering means", and is not compared to any signal generated by the cited diagnostic unit (i.e., the diagnostic unit does not generate a retrigger signal). Further, Applicant argues, regarding the cited "trigger" signal, the alleged correspondence to the claimed release signal is illogical because only a single trigger is generated, whereas the claimed invention is directed to the generation of two release signals that are compared; the cited diagnostic unit never retriggers, and instead uses the time pattern to determine

Art Unit: 2416

whether the bus monitor properly retriggers; so, Applicant argues, as only a single trigger is generated in the '805 reference, no comparison can be made as claimed in the instant application. As applicable to the rejection of claim 11, the cited "watchdog" thus also fails to compare any signals from the diagnostic unit, as the diagnostic unit does not generate a trigger. Moreover, Applicant argues, the cited retrigger and the time pattern (initial trigger) are not independently generated as the claimed release signals are, because the retrigger is actually based upon the time pattern (and initial trigger). Further, Applicant argues, the cited portions of the '168 reference do not provide correspondence to limitations directed to blocking network access based upon the coincidence (timing) of signals as asserted in the Office Action, which the Office Action acknowledges, but goes on to cite portions of the '168 reference as allegedly providing correspondence to these limitations. However, the cited "arbitration logic" 510 does not operate based upon any "coincidence" of signals, and is instead based upon matching identifications; Applicant cites, the "comparison circuit" 540 "compares device identification bits 535 to master identification bits 525," but this comparison has nothing to do with coincidental signals (i. e., has nothing to do with timing), making the cited ID comparison involves determining timing coincidence is untenable. Next, Applicant argues that the proposed combination of references is improper because the combination would render the '805 reference inoperable for its purpose because replacing the retrigger comparison of the '805 reference with an arbitration scheme based upon the ID of the bus agent sending the request would result in blocking or allowing bus access regardless of any timing-related conditions.

4. Examiner replies that, as cited, Belschner teaches of a network node comprising a communication unit for the implementation of a communication protocol for communication with other network nodes via a communication medium a bus monitor, and a bus driver, where the communication unit and the bus monitor each mutually independently and each implement an access time schedule contained in a configuration data record. Examiner relies on Kleveland to complement Belschner, in teaching the limitation of the event that when the two release signals do not coincide, of blocking the access of the

Art Unit: 2416

network node to the communication medium. Motivation to combine these two references is given in the Office Action.

5. Applicant further traverses the Section 103 rejections because the Office Action has failed to cite teaching or suggestion of limitations; in claim 3, the cited "element" 445 and 446 in the '289 reference does not appear to show any inverse coding as each "element" appears respectively to refer to a node at which an output 451 of a flip-flop 450 and a clock signal are provided. Generally, the rejection is vague and unclear as to what is being asserted as teaching or suggesting inversely-coded signals and, specifically, inversely-coded trigger signals as modified in the '805 reference; the cited portions of the '289 reference appear unrelated to the '805 reference and the Office Action's asserted.

6. Examiner replies that Riley is cited as exemplary to show that polarities of signals in VLSI are determined by the physical design, timing and performance specification of the logic.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

a. A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1, 11 – 12, and 17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Belschner, et al (U.S. Patent 7103805), in view of Kleveland (U.S. Patent 5528168)

9. With regards to claims 1, 12 and 17, Belschner teaches of a network node and device comprising a communication unit for the implementation of a communication protocol for communication with other network nodes via a communication medium a bus monitor, and a bus driver, where the communication unit and the bus monitor (2: [0046] read The bus monitor unit which is integrated into the central node is suitable for monitoring access of users to the data bus, without having to install the bus monitor unit in a

Art Unit: 2416

decentralized controller for this purpose. The central bus monitor unit i.e. bus monitor unit and the diagnostic unit i.e. communication unit can be used to prevent faulty access to the data bus by a user) each mutually independently; 3: [0030] read [t]he central node with the integrated diagnostic unit therefore forms a closed system which preferably also has fault-handling routines, so that the central node is operationally capable independently of external diagnostic units, and has its own fault detection means i.e. mutually independent.); each implement an access time schedule contained in a configuration data record (2: [0013] read For this purpose, a time-registering means i.e. access time schedule is provided which registers the time patterns of the data bus for the transmission of a user i.e. configuration data record and, triggered by these time patterns, assigns a transmission slot to each user.) and each make available, in accordance with the access time schedule, a release signal for the bus driver the bus driver evaluates these two release signals (3: [0013] read Based on the second time pattern made available to it, the diagnostic unit checks whether the bus monitor unit regularly retriggers in response to the time patterns by means of the trigger signals i.e. evaluates these two release signals).

10. However Belschner does not disclose in the event that the two release signals do not coincide of blocking the access of the network node to the communication medium

11. Kleveland teaches this limitation (10: [0030] read [a]rbitration logic 510 includes a temporary bus master identification register, master ID 520, coupled by master comparison bits 525 to comparison circuit 540. i.e. logic for blocking the access of the network node if two release signals do not coincide)

12. It would have been obvious at the time the invention was made to a person of ordinary skill in the art to modify the bus access teachings of Belschner with the comparison circuit teachings of Kleveland.

13. In this manner, access to data bus can be regulated in a discipline manner so as to mitigate user collisions on the data bus which would yield the system dysfunctional.

14. In regards to claim 11, Belschner teaches of a bus driver for a network node which is provided for communication with other network nodes via a communication medium and a bus driver that

Art Unit: 2416

evaluates two mutually independent release signals that implement an access time schedule to generate the release signals. (2: [0046] read The bus monitor unit which is integrated into the central node is suitable for monitoring access of users to the data bus, without having to install the bus monitor unit in a decentralized controller for this purpose. The central bus monitor unit i.e. bus monitor unit and the diagnostic unit i.e. communication unit can be used to prevent faulty access to the data bus by a user) each mutually independently; (5: [0006] read [t]he watchdog i.e. bus driver, monitors the cyclical synchronization of the bus monitor unit with the time patterns of the data bus i.e. evaluates two release signals for equality of the release information made available to it by two separate units for a communication medium, and switches the bus monitor unit to an inactive state when the trigger signal fails to occur, blocking or releasing the communication in a way which can be configured for all the users i.e. in the event that the release signals do not coincide, the bus driver blocks the access of the network node. And 3: [0030] read [t]he central node with the integrated diagnostic unit therefore forms a closed system which preferably also has fault-handling routines, so that the central node is operationally capable independently of external diagnostic units, and has its own fault detection means i.e. mutually independent.); and 2: [0013] read For this purpose, a time-registering means i.e. access time schedule is provided which registers the time patterns of the data bus for the transmission of a user i.e. configuration data record and, triggered by these time patterns, assigns a transmission slot to each user.) and each make available, in accordance with the access time schedule, a release signal for the bus driver the bus driver evaluates these two release signals and 3: [0013] read based on the second time pattern made available to it, the diagnostic unit checks whether the bus monitor unit regularly retriggers in response to the time patterns by means of the trigger signals i.e. evaluates these two release signals)

15. However, Belschner does not disclose where the bus driver evaluates two release signals for equality of the release information made available to it by two separate units.

Art Unit: 2416

16. Kleveland teaches this limitation (10: [0030] read [a]rbitration logic 510 includes a temporary bus master identification register, master ID 520, coupled by master comparison bits 525 to comparison circuit 540. i.e. logic for blocking the access of the network node if two release signals do not coincide or are not equal.)

17. It would have been obvious at the time the invention was made to a person of ordinary skill in the art to modify the bus access teachings of Belschner with the comparison circuit teachings of Kleveland.

18. In this manner, access to data bus can be regulated in a discipline manner so as to mitigate user collisions on the data bus which would yield the system dysfunctional.

19. Claims 3 – 10, 13, 15 – 16 and 18 – 20 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Belschner, et al (U.S. Patent 7103805), in view of Kleveland (U.S. Patent 5528168) and in further view of Riley et al (U.S. Patent 5706289).

20. With regards to claims 3, 15, and 19, Belschner, modified teaches of a network node as claimed in claim 1, characterized in that the release signals of the communication unit and the bus monitor, but does not teach that the signals are coded inversely to one another.

21. The polarities of signals in VLSI are determined by the physical design, timing and performance specification of the logic as shown in, for example, in Riley Figure 13 element 445 and 446.

22. It would have been obvious at the time the invention was made by a person of to having ordinary skill in the art to modify the teachings of Belschner, modified Riley so that release signals are coded inversely to one another if the design so dictated.

23. In this manner, the time slot of bus could be blocked or not in the most expedient manner per a specific set of physical specifications.

24. In regards to claims 4 – 5, 16, and 20, Belschner modified, teach a network node characterized in that the evaluation of the two release signals is undertaken in the bus driver, but does not teach the of the influence of a low-pass filter or of a low-pass filter of configurable design.

Art Unit: 2416

25. Riley teaches of the evaluation of the two signals is undertaken in the bus driver with the influence of a low-pass filter or of a low-pass filter of configurable design. (8: [0024] read shown in block form in FIG. 2A, the channel input signal at the channel A input terminal to the integrated circuit is fed through a dual signal conditioning circuit before further processing. The signal conditioning circuit includes a Channel A signal conditioning circuit (shown in FIG. 3A) i.e. configurable low-pass filter. As shown in FIG. 3A, the signal conditioning circuit 122 has an anti-aliasing filter, a hysteresis circuit, and a digital low pass filter.)

26. It would have been obvious at the time the invention was made by a person of ordinary skill in the art to modify the teachings of Belschner, modified Riley to condition the input release signal with a configurable low pass filter.⁶

27. In this manner, noise or channel transients can be mitigated thus improving the fidelity of the protection time slot logic for the bus.

28. In regards to claims 6 and 7, Belschner teaches that error-state detection generated in the bus driver is resettable from the outside and can be signaled to the outside. (4: [0056] read [t]he bus monitor unit is connected via an interface to a communications computer of the central node, which loads and calculates the time patterns i.e. access time schedule contained in a configuration data record, for the accepted transmission slots of the individual users i.e. communication nodes. The interface is a component of the configuration means).

29. Regarding claim 8, Belschner teaches that the bus monitor and the bus driver are integrated into one unit. (2: [0045] read the bus monitor unit is integrated into the central node is suitable for monitoring access of users to the data bus, without having to install the bus monitor unit in a decentralized controller for this purpose.).

30. In consideration of claim 9, Belschner teaches a network with network nodes where the network nodes communicate with each other via the communication medium. (Figure 1 element 6).

Art Unit: 2416

31. With regards to claim 10, Belschner teaches where redundant network channels are provided, wherein a bus monitor and a bus driver are assigned to each network channel in each network node (7: [0004] read FIG. 3 shows an example of a time pattern such as can be determined by the unit for setting the configuration parameters 21. First, two time slots are provided for the user 7, followed by a time slot for the third user 9. The two time slots which are represented in a hatched form are marked as blocked by the hatching, i.e. the bus monitor unit 5 has detected a faulty transmission signal at this time; as a result, the time slot is blocked both for transmission and reception. However, on the other hand, it would also be possible for signal filtering to take place so that the correct signal is generated by means of a filter or a redundant channel.).

32. In regards to claim 13 and 18, Belschner modified teaches the limitations of claim 12, but does not disclose where the bus driver evaluates the independently-generated release signals to ensure that both signals match one another to mitigate a network access condition resulting from an improperly-generated release signal.

33. Riley teaches where the bus driver evaluates the independently-generated release signals to ensure that both signals match one another to mitigate a network access condition resulting from an improperly-generated release signal. (6: [0061] read in mode one, during the first part of the time slot 65, data is placed on the data bus 46 by one or more input data link modules 32 and the data remains on the data bus 46 for the entire time slot i.e. both signals match one another. At the midpoint 64 of the time slot 65, the data on the data bus 46 is copied from the bus to output terminals 98 and 100 on at least one output data link module 32 for use by at least one output device 54. i.e. to mitigate a network access condition resulting from an improperly-generated release signal)

34. It would have been obvious at the time the invention was made by a person of ordinary skill in the art to modify the teachings of Belschner, modified Riley so that release signals are properly matched.

Art Unit: 2416

35. In this manner, the time slot of bus could be blocked and an improperly-generated release signal can be mitigated

36. Claims 2 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belschner, et al (U.S. Patent 7103805), in view of in view of Kleveland (U.S. Patent 5528168) and in further view of Baek et al (U.S. Patent 5680554)

37. In consideration of claims 2 and 14, Belschner, modified Riley teaches of a bus driver activating the transmission stage if there is no blockage of access to the communication medium present, but does not teach of transmission request signal to the bus driver.

38. Baek teaches of transmission request signal to the bus driver (4: [0054] read NRQ represents the basic unit of a data transmission request signal...)

39. It would have been obvious at the time the invention was made by a person of ordinary skill in the art to modify the teachings of Belschner, modified Riley with Baek.

40. In this manner, the bus driver will be enabled only when it has data to transmit thus minimizing collision with other bus drivers.

FINAL ACTION

41. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

42. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

Art Unit: 2416

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

43. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HENRY BARON whose telephone number is (571)270-1748. The examiner can normally be reached on 7:30 AM to 5:00 PM E.S.T. Monday to Friday.

44. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

45. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/H. B./
Examiner, Art Unit 2416

HB

/Brenda Pham/

Primary Examiner, Art Unit 2416